A MODIFIED SVPWM ALGORITHM PROVIDING SOLUTION TO CAPACITOR BALANCING PROBLEM IN DIODE-CLAMPED MLI IN THE ENTIRE MODULATION REGION

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ABSTRACT
This paper presents a modified SVPWM algorithm to control DC-link imbalances in the three-level NPC-MLI. The proposed scheme is a result of the blend of the techniques: Nearest Three Vector (NTV) and Selected Three Vector (STV). This scheme can maintain DC-link voltage within a specified tolerance value for any value of modulation index with a wide range of load variation. The results of the proposed scheme exhibits DC-link voltage variation within 0.25%, which is well below the acceptable limit. The scheme guarantees to achieve voltage balancing without any additional control. The benefits of the proposed solution over existing schemes are verified through the MATLAB simulation.

KEY WORDS
Neutral point fluctuation (npf); Neutral-point Diode-Clamped Multi Level Inverter (NPC-MLI); Space Vector PWM (SVPWM); MATLAB-Simulation.

1. Introduction
Multilevel inverters (MLI) were proposed by Nabae.A (Nabae. A. et al, 1981). Since then multilevel inverters have drawn interest in the electrical power industry in recent years. MLI offers a set of features that are well suited for HVDC transmission, reactive power compensating devices, power conditioning, active power filtering and so on (Marcelo et al, 2012; Saeedifard. M. et al, 2009; S.Busquets-Monge et al, 2004:). Multilevel inverters have been classified as Diode clamped inverter, Capacitor Clamped inverter, Cascaded MLI and Hybrid type inverter (Rodriguez, J.S et al, 2010). NPC-MLI in Figure 1 suffers from the DC-link imbalance problem due to the dc link capacitors; magnitude of this problem increases with the increase in number of levels. The DC-link imbalance degrades the operation of the inverter by increasing the voltage stress on the semiconductor devices, introducing harmonics and distorting the output voltage. The neutral point balance can be achieved by using an algorithm to switch the inverter with proper switching states such that the DC-link balancing is achieved. Josep Pou et al have used stationary feed forward SVPWM for DC-link balancing, in which the duty cycle calculations involved are more complex. A new modulation approach for complete control of DC-link balancing in 3-level 3-phase NPC VSI has been proposed based on the virtual vector concept, which guarantees the balancing of DC-link voltage for any load over the full modulation range (Jian-Yong ZHENG et al, 2010). However this method has only been implemented using carrier based PWM which involves the calculation of angles and trigonometric ratios. A complete control has been obtained in the 3-level 3-phase NPC inverter (Amit Kumar Gupta et al, 2007). This scheme fully dependants on modulation index and reference vector angle.

In this paper, a SVPWM Nearest Three Vector and Selected Three Vector (NSTV) strategy is proposed. The crux of the scheme is ingenious usage of Nearest Three Vector (NTV) and the Selected Three Vector (STV) to bring the DC-link voltage fluctuations below the tolerated value. The presented solution is capable of eliminating the low frequency dc-link capacitor voltage oscillations and guarantees balancing of dc-link voltage in 3-level NPC-MLI over the full range of modulation. The improvement in npf through proposed SVPWM is much pronounced for higher modulation range than the lower. The scheme is simulated and conceptual feasibility is thoroughly understood using MATLAB software.

2. Traditional Space Vector PWM Strategy
The SVPWM treats sinusoidal voltage as constant amplitude vector rotating at constant frequency with reference voltage vector \( \mathbf{V}^* \), defined by \( \mathbf{V}^* = |\mathbf{V}^*| e^{j\omega t} \), rotates around the centre of the space vector (SVM) diagram at an angular frequency \( \omega = 2\pi f_{sys} \) (e.g. \( f_{sys} = 50 \) Hz). The 3-phase 3-level space vector diagram illustrated in Figure 2 The rotating reference vector \( \mathbf{V}^* \) lies in any of the sectors inside that 4 sub-triangles are available. The three vectors of the corresponding triangle can be used to synthesise the sampled reference voltage vector.
The algorithm for multi-level SVM is to be implemented by the following steps: Location of the sector and the triangle in which the tip of the reference vector lies; Selection of the adjacent switching vectors; Calculation of the duty cycles of the switching vectors; Calculation and application of the switching pattern.

\[ V^*\delta_{s1} + V^*\delta_{s2} + V^*\delta_{M1} = V^* \]  
\[ \delta_{s1} + \delta_{s2} + \delta_{M1} = 1 \]

The algorithm for multi-level SVM is to be implemented by the following steps: Location of the sector and the triangle in which the tip of the reference vector lies; Selection of the adjacent switching vectors; Calculation of the duty cycles of the switching vectors; Calculation and application of the switching pattern.

3. Influence of Switching Vector for DC-Link Imbalance

3.1 DC-link capacitor balancing problem with respect to phase current

While using large and zero vectors the phase currents become zero and hence the balance could be obtained. DC-link imbalance is mainly due to medium vectors, because the phase currents are not zero in those vectors (Katsutoshi Yamanaka) as indicated in Table.1. In the \( \Delta_2 \) without redundant switching states, the phase currents are available in switching states \((-i_a+i_c+i_b)\). Due to the existing phase currents, DC-link capacitor balance cannot be achieved. The Table.1 shows the balanced and influenced vectors for DC-link imbalance. The capacitor can be balanced by proper utilization of the short, zero and large vectors without using the medium vectors (du Toit Mouton H et al, 2002).

![Figure 1. Circuit diagram for 3-level NPC-MLI](image1)

3.2 DC-link capacitor balancing problem with respect to modulation index

For the linear modulation region, there are three modes; (i) \( 0 \leq m < 0.5 \) in this mode, the active vectors are the short vectors and the balance is achieved undoubtedly, (ii) \( 0.5 \leq m < 0.8 \) the active vectors are medium and short vectors, where balancing becomes poor and (iii) in higher modulation index \( 0.8 \leq m < 0.907 \), the participation of the medium vector is maximum and it can compensate the short vector as the DC-link capacitor imbalance is high. At higher modulation index, the reference vector lies in \( \Delta_1, \Delta_2 \) and \( \Delta_3 \) and results in imbalance. The Figure 2 shows that npf against various triangles and it is evident that higher range of output, inherits magnified dc link imbalance.

![Figure 2. Space Vector Diagram of NPC-MLI](image2)

4. Modified Switching Vector Scheme to Reduce the D.C-Link Imbalance

The major problem in the neutral point diode clamped inverter is D.C-link balancing. The D.C-link balancing can be defined as \[8\] .

\[
\text{Percentage of D.C-link imbalance} = \frac{(V_{dc-link}/n-1 - V_{c2})}{V_{dc-link}/n-1} \times 100 \%
\]

where \( n \) is number of levels, \( V_{dc-link} \) is applied dc voltage and \( V_{c2} \) is capacitor voltage

The issues of the D.C-link balancing problem can be rectified by controlling the movement vector in circular position. The nearest three vector (NTV) scheme is used to switch the vertices of the triangle in every switching period for the modulation index below \( (0.5 \leq m < 0.5) \) it gives better performance. At the modulation index \( (0.5 \leq m < 0.907) \) there is the large fluctuation due to participation of the medium vector it can lead to large D.C-link imbalance problem. The selected three vectors (STV) will reduce the D.C-link imbalance problem at the higher modulation index.
TABLE 1
Phase currents according to sector 1

<table>
<thead>
<tr>
<th>Δ</th>
<th>ZERO VECTORS</th>
<th>SHORT VECTORS</th>
<th>MEDIUM VECTOR</th>
<th>LARGE VECTOR</th>
<th>INFLUENCE VECTOR</th>
<th>BALANCING VECTOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Δ₀</td>
<td>[000]0-[111]0-<a href="0">1-1-1</a></td>
<td>[100][i₁][0-1-1] (i₃)</td>
<td>[10-1][i₃]</td>
<td><a href="0">11-1</a></td>
<td>Medium vector</td>
<td>Short vectors</td>
</tr>
<tr>
<td>Δ₁</td>
<td>-</td>
<td>[100][i₃][0-1-1] (i₃)</td>
<td><a href="i%E2%82%83">10-1</a></td>
<td>-</td>
<td>Medium vector</td>
<td>-</td>
</tr>
<tr>
<td>Δ₂</td>
<td>-</td>
<td>[100][i₃][0-1-1] (i₃)</td>
<td>[10-1][i₃]</td>
<td>-</td>
<td>Medium vector</td>
<td>-</td>
</tr>
<tr>
<td>Δ₃</td>
<td>-</td>
<td>[110][i₃][00-1] (i₃)</td>
<td><a href="i%E2%82%83">10-1</a></td>
<td><a href="0">11-1</a></td>
<td>Medium vector</td>
<td>-</td>
</tr>
</tbody>
</table>

4.1 Nearest Three Vector (NTV) scheme

The nearest three vector (NTV) scheme is used for the D.C-link balancing without using the middle vector. Figure 3 shows the reference is located in the triangle Δ₁. The switching vectors V_S1, V_M, V_L are switched and the corresponding states are (0-1-1), (1-1-1), (10-1) and (100).

![Figure 3. Sector 1 for NTV scheme](image)

The triangle in the sector is considered as a sector of virtual two level inverter. The sector where the control vector is located can be identified by the Δ₀ by the general implementation of the space vector modulation scheme. Using the reference point the suitable vertex of the triangle can be taken as the zero vector of the two level sector. The duty ratios are

\[ \delta_a = \frac{V_{ref}V_p}{\sqrt{3}} \]  
\[ \delta_b = \frac{V_p}{m} \]  
\[ \delta_c = 1 - \delta_a - \delta_b \]

4.2 Selected Three Vector (STV) scheme

The space vector consists of 6 sectors in each sector 4 sub triangles. The sub triangles can be split into 6 triangles by joining V_L2 and V_S2, V_S1 and V_L1, and V_Z and V_M, so that the triangles are named as Δ₅(V_{L2}, V_{S2}, V_{Z}), Δ₆(V_{S1}, V_{L2}, V_{Z}), Δ₇(V_{S1}, V_{L1}, V_{S2}), Δ₈(V_{S1}, V_{L1}, V_{L2}), Δ₉(V_{S2}, V_{L1}, V_{L2}), and Δ₁₀(V_{L2}, V_{S1}, V_{S2}). In Figure 4 only the short and long

are used, the medium vectors are neglected to reduce D.C. link imbalance.

In the triangle splitting the centre point Vₜ is considered as the midpoint, that point will produce the zero phase current according to the nearest three vector (NTV) scheme that figure has been shown below. In this Vₜ must be zero so according to this method the ground point will not lead to D.C-link imbalance.

\[ V_{\delta t} = \frac{1}{3} (V_{S1} (110) + V_M (101) + V_{S1} (110)) \]  

Triangle determination:

If the reference V* is below the 30°, then V* may be in the Δ₅ or Δ₆. Then the magnitude of the reference point is divided in the ratio 2:1 when the reference point satisfies \( V_a + \sqrt{3} V_\beta \leq 2 \) the point must be in Δ₅, otherwise in Δ₆. If the reference V* is above the 30°, then V* may be in Δ₇ or Δ₉. Then the magnitude of the reference point is divided in the ratio 1:2 when the reference point \( V_a \geq 1 \) the point must be in Δ₇, otherwise in Δ₉.

On time calculations

The reference point lies in the triangle Δ₅ if both the inequalities \( \alpha \leq 30° \) and \( V_a + \sqrt{3} V_\beta \leq 2 \) are satisfied

\[ \delta_{V_{S1}} = 2 \cdot V_a + \sqrt{3} \cdot V_\beta \]  
\[ \delta_{V_{S2}} = \frac{V_p}{m} \]  
\[ \delta_{V_{S2}} = 1 - \delta_{V_{S1}} - \delta_{V_{S2}} \]

Similarly the duty ratios are calculated for the remaining triangles.
TABLE 2
Proposed Selected Vector SVPWM Scheme For 3 Level NPC-MLI

<table>
<thead>
<tr>
<th>SECTOR</th>
<th>REGION</th>
<th>VECTORS</th>
<th>LARGE VECTOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>∆(V_S1, V_L1, V_S2)</td>
<td>[100][-i_a]-[0-1-1] (i_a), <a href="i_a">110</a>-[0-1-1] (-i_c)</td>
<td><a href="0">1-1-1</a></td>
</tr>
<tr>
<td></td>
<td>∆(V_S1, V_L2)</td>
<td>[100][-i_a]-[0-1-1] (i_a)</td>
<td><a href="0">1-1-1</a>-<a href="0">11-1</a></td>
</tr>
<tr>
<td></td>
<td>∆(V_S2, V_L1, V_L2)</td>
<td>[110][i_a]-[00-1] (-i_a)</td>
<td><a href="0">1-1-1</a>-<a href="0">11-1</a></td>
</tr>
<tr>
<td></td>
<td>∆(V_S1, V_S2, V_L2)</td>
<td>[100][-i_a]-[0-1-1] (i_a), [110][i_a]-[0-1-1] (-i_c)</td>
<td><a href="0">11-1</a></td>
</tr>
</tbody>
</table>

The Table 2 shows the Selected Three Vector (STV) switching states with their corresponding currents for a three level NPC MLI.

While using the short vectors with a redundant state, the phase currents [100][-i_a]-[0-1-1] (i_a) become zero and large vector has zero phase current. So capacitor is not influenced by any phase current. The below Table 3 shows the switching vectors for the NTV and STV schemes.

TABLE 3
Proposed SVPWM

<table>
<thead>
<tr>
<th>∆SUB</th>
<th>NTV</th>
<th>STV</th>
</tr>
</thead>
<tbody>
<tr>
<td>∆_1</td>
<td>V_{Z0} V_{S1} V_{S2}</td>
<td>V_{Z0} V_{S1} V_{S2}</td>
</tr>
<tr>
<td>∆_2</td>
<td>V_{S1} V_{L1} V_{S2}</td>
<td>-</td>
</tr>
<tr>
<td>∆_3</td>
<td>V_{S2} V_{M1} V_{L2}</td>
<td>-</td>
</tr>
<tr>
<td>∆_4</td>
<td>V_{S1} V_{M1} V_{L1}</td>
<td>-</td>
</tr>
<tr>
<td>∆_5</td>
<td>-</td>
<td>V_{S1} V_{S2} V_{S}</td>
</tr>
<tr>
<td>∆_6</td>
<td>-</td>
<td>V_{S1} V_{L1} V_{S2}</td>
</tr>
<tr>
<td>∆_7</td>
<td>-</td>
<td>V_{S1} V_{L1} V_{L2}</td>
</tr>
<tr>
<td>∆_8</td>
<td>-</td>
<td>V_{S2} V_{L1} V_{L2}</td>
</tr>
<tr>
<td>∆_9</td>
<td>-</td>
<td>V_{L2} V_{S1} V_{S2}</td>
</tr>
</tbody>
</table>

5. Implementation of Proposed Algorithm

The general SVM scheme of 3-level inverter and timing calculations implementation are carried out based on the 2-level inverter. In this, the NTV and the STV schemes are incorporated based on these switching selections. If the DC-link imbalance is more than the maximum level, the STV scheme is used and whenever it is less than the maximum level, NTV scheme is used. Alternatively if the modulation index is greater than 0.6 then due to the contribution of the medium vectors the vector moves in...
such a manner that only the short vectors can be used which leads to the usage of the STV scheme. The following flow chart in Figure 6 describes the switching selection in more details.

Figure 6. Flow chart for Proposed NSTV Scheme

6. Simulation Results

The performance of the proposed (NTV and STV) algorithm for space vector modulation have been investigated and simulated by MATLAB 11.b for 12 switch neutral point diode clamped MLI with 300V DC-link, two 100 micro Farad capacitor, 5kHz switching frequency fed 1 HP squirrel cage 3 phase induction motor open loop v/f control drive. Figure 7 (a) shows the line to line voltage for NTV scheme. The Figure 7(b) shows the Capacitor voltage imbalance using the NTV scheme at 0.9 modulation index; the capacitor voltage $V_{c2}$ is about 91.9V. Hence using Eq.(3), the npf value of 3.7% is obtained. Figure 7(c) shows the line voltage for Proposed NSTV scheme.

Figure 7(d) shows voltage across the capacitor using proposed NSTV scheme for the same modulation index 0.907, which results the npf values as 0.22%. Here the proposed NSTV scheme limits the DC-link imbalance value to 0.22 %, which is well below the IEEE standard requirement of 1% (Nomura s et.al,2005).
Figure 8. Simulation result in Matlab 11. b for three level inverter with Modulation Index = 0.7, f = 50Hz, C₁ = C₂ = 100 micro farad: DC link capacitor voltages V₁ and V₂ [1 V/div], for Proposed NSVT –SVM scheme with 0.212 % npf.

The performance analysis of NPC-MLI under Conventional SVM, NTV & proposed NSTV schemes have been carried out and the results are tabulated at different values of modulation index for easy reference as follows:

**TABLE 5**  
npf, Line voltage & Harmonic analysis at mᵢ = 0.6

<table>
<thead>
<tr>
<th>SVM Schemes</th>
<th>npf %</th>
<th>V⁻line</th>
<th>THD %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>4.5</td>
<td>160.5 V</td>
<td>12.2</td>
</tr>
<tr>
<td>NTV-SVM</td>
<td>2.08</td>
<td>169.6 V</td>
<td>10.56</td>
</tr>
<tr>
<td>Proposed NSTV</td>
<td>0.202</td>
<td>166.8 V</td>
<td>10.43</td>
</tr>
</tbody>
</table>

**TABLE 6**  
npf, Line voltage & Harmonic analysis at mᵢ = 0.7

<table>
<thead>
<tr>
<th>SVM Schemes</th>
<th>npf %</th>
<th>V⁻line</th>
<th>THD %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>4.9</td>
<td>191.0 V</td>
<td>14.50</td>
</tr>
<tr>
<td>NTV-SVM</td>
<td>2.25</td>
<td>199.0 V</td>
<td>10.62</td>
</tr>
<tr>
<td>Proposed NSTV</td>
<td>0.21</td>
<td>196.8 V</td>
<td>10.23</td>
</tr>
</tbody>
</table>

**TABLE 7**  
npf, Line voltage & Harmonic analysis at mᵢ = 0.907

<table>
<thead>
<tr>
<th>SVM Schemes</th>
<th>npf %</th>
<th>V⁻line</th>
<th>THD %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>5.2</td>
<td>260.0 V</td>
<td>14.70</td>
</tr>
<tr>
<td>NTV-SVM</td>
<td>2.8</td>
<td>268.9 V</td>
<td>10.76</td>
</tr>
<tr>
<td>Proposed NSTV</td>
<td>0.22</td>
<td>266.9 V</td>
<td>10.42</td>
</tr>
</tbody>
</table>

Here, the range of modulation index (0<mᵢ<0.5),the value of THD% can be easily maintained by using the NTV scheme.However if the modulation index goes beyond the 0.5 (mᵢ>0.5),due to the participation of the medium vectors the npf and THD increases which are not to be acceptable Therefore for the modulation index (mᵢ≥0.5), the STV scheme is used to limit the npf.

The Table 5 to Table 7 shows the conventional, NTV and STV SVM schemes for different modulation index and the corresponding values of npf%, output line voltages and the percentage of THD. The Table 6 shows the values of npf%=5.2% and THD%=14.70% which are
considered to be high, at modulation index 0.907 using the existing SVM scheme.

Figure 10. % of DC-link imbalance verses Modulation index for Proposed (NTV+ STV) schemes

So in order to reduce those values, Nearest three vector scheme was implemented where the npf% was reduced to 2.8% and THD% to 10.76% with an additional advantage of increase in line voltage with the involvement of medium vectors. The %npf was further reduced to 0.22% by using the NSTV SVM scheme and the %THD = 10.42% was also reduced. Therefore the proposed NSTV SVM scheme without using the medium vectors reduces the percentage of npf to 0.22% (which is well below the IEEE standards) and the THD% reduced to 10.42% and also the NSTV scheme maintains the good power factor. However, the line voltage obtained was somewhat lesser than the NTV scheme. The Figure 10 spectacles the three dimentional chart about npf %, Line voltage and THD % verses different modulation index of both the NTV and NSTV SVM schemes. At this juncture, we can understand through out the entire modulation range the proposed NSTV –SVM scheme maintains the npf up to 0.2% with less THD

6.1 Analysis of CMV depending upon switching states

The proposed SVM scheme is better to balancing capacitor, but to consider the Common mode voltage it will producing 33% \( V_{dc} \), which is same as conventional. It can be reduced by choosing the proper Switching events.

The common mode voltage is defined as the voltage between star connected load neutral point and ground of the inverter. It is given as[12]

\[ V_{ng} = \frac{(V_{an} + V_{bn} + V_{cn})}{3} \]  

(11)

The common mode voltage is mostly depend upon the average of the inverter phase voltages. In the star connected load sum of the phase voltage must be zero. Here in the 3-level npc inverter produce different combinations of phase voltages depend upon the switching states available in the SVPWM[13]. In the conventional SVPWM the state 1 produce \( +V_{dc}/2 \), 0 produces 0V & -1 produce \(-V_{dc}/2 \). In the operation of the conventional SVPWM has 27 switching states each state has different CMV[14][15]. According to the detailed analysis, 12 switching states produce \( \pm V_{dc}/6 \), 7 states produce zero CMV, 6 states produce \( \pm V_{dc}/3 \) & 2 states produce \( \pm V_{dc}/2 \) as shown in Table 8.

<table>
<thead>
<tr>
<th>Group</th>
<th>Switching states of 3–level inverter</th>
<th>CMV</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>111</td>
<td>( V_{dc}/2 )</td>
</tr>
<tr>
<td>B</td>
<td>110, 101,111</td>
<td>( V_{dc}/3 )</td>
</tr>
<tr>
<td>C</td>
<td>1–11, 11–1, –111, 001, 010, 100</td>
<td>( V_{dc}/6 )</td>
</tr>
<tr>
<td>D</td>
<td>000, 01–1, 0–11, 10–1, 1–10, –101, –110</td>
<td>0</td>
</tr>
<tr>
<td>E</td>
<td>–1–11, –11–1, 1–1–1, 00–1, 0–10, –100</td>
<td>( –V_{dc}/6 )</td>
</tr>
<tr>
<td>F</td>
<td>10–1, 0–1–1, 0–1, 1–1–1</td>
<td>( –V_{dc}/3 )</td>
</tr>
<tr>
<td>G</td>
<td>–1–1–1</td>
<td>( –V_{dc}/2 )</td>
</tr>
</tbody>
</table>

The proposed NSTV-SVM scheme will produce common mode voltage equal to \( +V_{dc}/3 \) as like conventional SVPWM and the value of the common mode voltage can be reduced by proper switching schemes[16]. The Fig 11 shows the CMV developed in an induction motor when connected to a three level diode clamped inverter. The inverter is controlled by the Proposed NSTV technique with a carrier frequency of 1050 Hz and a modulating index of 0.9.

Fig.11 Common mode voltage of three level NPC inverter

In addition to this, the same NSTV - SVM scheme can be extened to over modulation region (modulation index
more than 0.907) with small changes in duty cycle calculations and vector participation.

The proposed PWM scheme, similar to other control approaches, utilizes a redundant active vector in a switching sequence in order to reduce the dc link voltage balance. The main difference is in selecting the methods of three nearest selected vector with redundant state.

The salient features of the proposed scheme are,

✓ The scheme is able to maintain DC-link balance within a specified tolerance value with any modulation index and for wide load variation. Hence, large DC-link capacitors are not required.
✓ DC-link voltage fluctuation is the only feedback parameter required to obtain overall good performance, no additional input is required.
✓ The volt-sec balance is maintained throughout the scheme.

The scheme is computationally simple and hence can be easily implemented.

7. Conclusion

A novel SVPWM modulation approach for control the DC-link voltage in the three-phase three-level NPC VSI is presented. The proposed NSTV scheme maintains the DC-link imbalance within a specified tolerance value. The balancing of the DC-link voltage is achieved irrespective load condition (current magnitude, power factor etc.) and over the full range of inverter output voltage. Thus, the proposed NSTV scheme limits the DC-link imbalance value to 0.25%, which is well below the IEEE standard requirement of 1% (Nomura S et al, 2005). The scheme significantly reduces the size of the dc-link capacitors and maintains the volt-sec balance throughout the working range.

References