ABSTRACT
This paper describes a single stage fully differential folded cascode operational transconductance amplifier (OTA) with fully differential gain boosting amplifiers designed in 1.2 VDC 130nm CMOS process technology. The amplifier is the driver for the analog to digital converter (ADC) of a blood pressure sensing medical implant [1] which uses wireless power transmission as its energy source [2]. The medical implant’s design specifications require an amplifier with wide output swing, high accuracy, and the bandwidth to drive a differential 5 pF load at 4 ksps with minimum power consumption. The gain boosting amplifiers are telescopic cascoded amplifiers, which, by their design, have an input and output common mode voltage relationship which is opposite to what is needed for a gain boosted cascode configuration. To correct for this, a method for DC shifting the amplifier’s input voltage using a switched capacitor network is presented.

KEY WORDS
Biomedical Electronics, Electronic Medical Devices, Biosensors and transducers, Data and Signal Acquisition.

1 Introduction
ADC drivers require very high accuracy to meet the settling requirements of the signal conditioning circuitry, and the amplifier’s accuracy is determined by its open loop DC gain. High gain can be achieved using a multistage amplifier, but the main drawback is the greatly increased power consumption incurred by each successive amplifier stage. Another option for increasing the DC gain is to implement a gain boosted cascode stage as the amplifier’s output load.

The amplifier for this wireless medical implant has been designed to provide very large DC gain over a wide output swing, and to consume an absolute minimum of power. Towards the goal of achieving wide output swing, a folded cascode architecture is used which allows the output node voltages to approach the power supply rail potentials (minus the saturation voltages, $V_{dsat}$, of the load devices). To achieve very high DC open loop gain, the gain enhancement effect of a folded cascode architecture is further increased by adding an extra amplifier to drive the gates of the cascode devices. To keep the overall system power consumption low, all of the system’s amplifiers (the main folded cascode OTA and the gain boosting OTAs) are single stage designs employing switched capacitor common mode feedback networks.

2 Folded Cascode Design
The system’s folded cascode OTA, without the gain boosting amplifiers, is given in Figure 1. To design for the system bandwidth and settling requirements, the amplifier’s closed loop time constant $\tau$ is derived with regard to the required accuracy, $\epsilon$, and settling time, $t_s$. From $\tau$, the input device’s transconductance $g_{m1}$ can be determined with regard to the amplifier’s closed loop feedback factor $F$ and the effective load capacitance $C_{\text{eff}}$ (1).

$$
\epsilon = e^{-\frac{\tau}{t_s}}
$$

$$
\tau = \frac{C_{\text{eff}}}{R_{\text{eff}}} = \frac{C_{\text{eff}}}{F}
$$

$$
g_{m1} = -\frac{\ln(\epsilon) C_{\text{eff}}}{t_s F} \quad (1)
$$

Figure 1. The folded cascode amplifier without the gain boosting amplifiers.
2.1 Noise Factor Design

The OTA noise requirements are fulfilled through the use of the noise factor, \(nf\), design variable which is used to scale the M1 input device input referred noise voltage to the total OTA input referred noise voltage. The transistors which contribute to an output node’s total noise current are the input device, M1, and load transistors, M2 and M5, with the cascode devices, M3 and M4, contributing a relatively insignificant amount of noise (see Sec. 4.3).

\[
V_{\text{noise,\text{in}}}^2 = 4kT \frac{\gamma_1}{gm_1} \tag{2}
\]

M1’s input referred noise voltage is given as (2) where the \(\gamma\) factor, which for this design has been determined through Spectre noise simulations (Figure 12), is used to relate the transistor’s \(\frac{1}{gm}\) value to an effective noise resistance as a function of the device transconductance efficiency \(\eta\) (6). A MOSFET has different noise characteristics depending on its region of operation. Using the simulation data collected in Figure 12 allows the output noise current to be determined with a smooth transition between the thermal noise characteristics for the devices operating in strong saturation [3] to the shot noise characteristics from the devices operating in subthreshold region [4]. The total OTA output noise current is a summation of the \(4kT\gamma gm\) noise currents from the noise generating transistors (3).

\[
I_{\text{noise,\text{in}}}^2 = 4kT \left(\frac{\gamma_1gm_1 + \gamma_2gm_2 + \gamma_5gm_5}{gm_1}\right) \tag{3}
\]

The total output noise current can be input referred by dividing it by the input device’s \(gm_1^2\) to get the OTA’s input referred noise voltage (4).

\[
V_{\text{noise,\text{in}}}^2 = 4kT \frac{\gamma_1}{gm_1} \left(1 + \frac{\gamma_2gm_2}{\gamma_1gm_1} + \frac{\gamma_5gm_5}{\gamma_1gm_1}\right) \tag{4}
\]

The input device input referred noise voltage, (2), can be scaled to the OTA’s total input referred noise voltage, (4), through the use of the noise factor \(nf\) (5).

\[
V_{\text{noise,\text{in}}}^2 = 4kT \frac{\gamma_1}{gm_1} nf \tag{5}
\]

The metric used for sizing the MOSFET devices for this design is their transconductance efficiency ratio, \(\eta gm\) (6). With a bit of manipulation, the noise factor \(nf\) can be represented in terms of \(I_d, \gamma, \text{ and } \eta gm\) (7).

\[
\eta gm = \frac{gm}{I_d} \tag{6}
\]

\[
I_d = I_{d1} + (I_{d2} \gamma_2 \eta gm_2 \gamma_1 \eta gm_1) + (I_{d3} \gamma_3 \eta gm_3 \gamma_1 \eta gm_1) \tag{7}
\]

3 The Gain Boost Amplifiers

The output impedance of the folded cascode (with no gain boosters) from Figure 1 is \(R_{\text{ocasn,\text{folded}}} = (1 + gm_3r_0)r_{02} + r_{02}\) which can be approximated to (8), and the folded cascode amplifier open loop DC gain is (10).

\[
R_{\text{ocasn,\text{folded}}} \approx gm_3r_0r_{02} \tag{8}
\]

\[
R_{\text{ocasn,\text{folded}}} \approx gm_4r_{04}\tag{9}\]

\[
A_{\text{folded}} = \frac{gm_1}{R_{\text{out,\text{folded}}}^2} \tag{10}
\]

Adding gain boosting amplifiers to the Figure 1 folded cascode results in the circuit in Figure 2. The gain boosters work to keep the M5 (M2BC) drain voltages equal by applying gate biasing to M4 (M3BC). The gain boosting amplifiers increase the standard cascode output impedance (9) by a factor of \(A_{\text{ocasn}} + 1\), approximated to \(A_{\text{ocasn}}\) (11), where \(A_{\text{ocasn}}\) is the open loop gain of the corresponding P or N gain boosting amplifier. This results in a total gain boosted cascode amplifier gain of (13)
When the gains of the two gain boosters are equal, then the output impedance of the gain boosted amplifier is the output impedance of the folded cascode multiplied by $A_{oGB}$ (14). This makes the total gain (15), and combining (10) and (15) results in (16).

$$R_{outGB} = R_{outfolded}(A_{oGB})$$

$$A_{total} = gm_1 R_{outGB}$$

$$A_{total} = A_{folded}(A_{oGB})$$

### 3.1 Gain Booster Stability

For stability, the gain boosting amplifiers are designed so that their gain bandwidth product ($GBW_{GB}$) is greater than the closed loop bandwidth of the folded cascode amplifier ($BW_{folded}$) (17), and less than the transition frequency $f_{T}$ (18) of the corresponding cascode device which it is driving (19) [5] (either M3BC or M4 from Figure 2).

$$F = \text{Feedback Factor}$$

$$BW_{folded} = \frac{gm_1 F}{2\pi C_{load}}$$

$$f_{T4} = \frac{gm_{24}}{2\pi C_{gs4}}$$

$$BW_{folded} < GBW_{GB} < f_{T4}$$

### 4 Gain Boost Input Level Shifter

The gain boosting amplifiers are the telescopic cascode amplifiers from Figure 4. Telescopic cascode amplifiers consume 50% less current than a folded cascode design with equivalent gain and bandwidth parameters. However, a telescopic design has some severe limitations concerning the output voltage swing and the input to output common mode voltage relationship. Considering the GB_N boost network from Figure 2, GB_N’s output node potential must be at least $V_{gsN}$ greater than its input node potential. However, looking at Figure 4, GB_N’s input devices will come out of saturation as the output node voltage approaches and exceeds the input voltage potential.

To correct for this, GB_N’s input voltage is level shifted up to a voltage which allows the amplifier to remain in saturation. The SC shifter in Figure 5 applies a DC shift from M2’s drain to GB_N’s input.

$$F_{GB} = \frac{C_{sc} + C_d}{C_{sc} + C_d + C_{par}}$$

The gain boosted amplifiers from Figure 4 have an open loop gain which is given as $A_{0GB}$. However, when the SC level shifter is used, then the effective gain of the
The SC level shifter in Figure 6 uses a deglitch capacitor in a reduction of the total amplifier gain to (22).

\[ \frac{C}{V} \text{input gate capacitance, and even in the extreme case where } \frac{C}{V} \text{capacitor up to } \frac{C}{V} = 2 \text{ and it uses non-overlapping clocks to charge the deglitch capacitor up to } V_{\text{C}_d} = \text{ref}_{\text{hi}} - \text{ref}_{\text{lo}} \text{. The symmetric dual } S_x \cdot C_{sc_x} \cdot S_x \text{ networks are SC resistors which supply charge to } C_d \text{ twice every SC clock period } T_{sc}, \text{ and the whole network acts as a switched capacitor } RC \text{ low pass filter with an RC time constant } \tau \text{ (24). From (24), } C_d + C_{cs} \text{ can be sized to meet the system's startup requirements.} \]

\[ \tau = \frac{C_d \cdot T_{sc}}{C_{sc} \cdot 2} \tag{24} \]

After the system’s capacitors have been sized according to (20), (23), and (24), then the switches can be sized so that their static on resistance is small enough that the poles which they introduce are at a high enough frequency not to interfere with the normal operation of the amplifier.

### 4.3 Gain Boosted Network Noise Current

The noise current of the gain boosted cascode can be analyzed using Figure 8 with the input referred noise voltages of the different devices. The input referred noise voltages of M1 and M5 are \( 4kT \gamma_{m1} \) but the input noise voltage on M4 is the summation of its own \( 4kT \gamma_{m4} \) noise plus GB_P’s output noise voltage (25).

\[ V_{\text{in}4}^2 = 4kT \frac{\gamma_{m4}}{g_{m4}} + 4kT \frac{\gamma_{m1}}{g_{m1}} \frac{n_f_{GB}}{F_{GB}} \]

\[ V_{\text{in}4}^2 = 4kT \frac{\gamma_{m4}}{g_{m4}} \left( 1 + \frac{g_{m4}}{\gamma_{m4}} \frac{n_f_{GB}}{F_{GB}} \right) \tag{25} \]

To get the noise current from M4, consider that M4 acts as a source follower, and because its \( I_d \) is set by M5, then \( V_{gs4} \) must remain constant. If \( V_{gs4} \) is constant, then M4’s source voltage is equal M4’s input referred noise voltage, which means that the output noise current from M4 is its input referred noise voltage divided by the parallel combination of M1 and M5’s load resistances (26). Summing M1, M5, and M4’s noise currents gives the total noise current for the P-side of the gain boosted folded cascode amplifier (27).

\[ I_{\text{out}4}^2 = \frac{V_{\text{in}4}^2}{(r_0 || r_{0b})^2} \tag{26} \]

\[ I_{\text{out}4}^2 = 4kT(\gamma_{m1} + \gamma_{m5}) + \frac{V_{\text{in}4}^2}{(r_0 || r_{0b})^2} \tag{27} \]
Dividing (27) by $g_m^2$ will give the total gain boosted folded cascode input referred noise voltage (28).

$$V_{in}^2 = 4kT \frac{\gamma_1}{g_m} \left( 1 + \frac{\gamma_5 g_m}{\gamma_1 g_m} + \frac{\gamma_4}{\gamma_1 g_m} \left( 1 + \gamma_4 \frac{g_m}{g_m g_m} \frac{V_{fb}}{V_{PP}} \right) \right)$$

(28)

From (28), the term $g_m g_m (r_{o1}/|r_{o2}|)^2$ is roughly one fourth of the transistor’s intrinsic $g_m r_{o}$ gain squared. Even in the extreme case where the $\gamma_{15}/\gamma_4$, the $g_m g_m$/$g_m g_m$, and the $\gamma_4/g_m$/$g_m g_m$ ratios are very poorly proportioned, $g_m g_m (r_{o1}/|r_{o2}|)^2$ should be large enough to make (29) true, thereby minimizing the impact of the cascode noise current source (30).

$$1 + \frac{\gamma_5 g_m}{\gamma_1 g_m} \gg \frac{\gamma_4}{\gamma_1 g_m} \left( 1 + \gamma_4 \frac{g_m}{g_m g_m} \frac{V_{fb}}{V_{PP}} \right)$$

(29)

$$V_{in_{narrow}}^2 \approx \frac{4kT}{g_m} \left( 1 + \frac{\gamma_5 g_m}{\gamma_1 g_m} \right)$$

(30)

5 Switched Capacitor Networks

To help reduce the system’s current consumption, switched capacitor networks are used to generate the system’s dynamic bias voltages $V_{cmfb}$ and $V_{float}$. The SC level shifter in Figure 9 generates the DC offset which biases M4’s gate to a potential which ensures that the amplifier remains in saturation, and the SC-CMFB block generates the common mode feedback voltage $V_{cmfb}$.

Figure 9. The SC level shifter is used to generate the floating cascode gate bias of the telescopic gain boosting cascodes.

Fully differential amplifiers require a defined output common mode voltage, and the circuit from Figure 10 [6] is used to generate the $V_{cmfb}$ bias voltage. The circuit operates by storing $(V_{ocm} - V_{flat})$ across the $C_{cs1}$ capacitors, and then connecting the $C_{cs2}$ capacitors differentially to the amplifier output nodes with the middle node $V_{cmfb}$ applying the corrective feedback voltage to the common mode feedback transistor.

Figure 10. The SC common mode feedback voltage generator [6].

6 Device Sizing

For this system, the medical implant design specifications require an amplifier with a thermal noise factor $nf$ less than or equal to 3.6. The amplifier will have a feedback factor of $F = \frac{1}{20}$, and it will be driving a differential load capacitance of $5pF$ (note that the 5 pF differential load $C_{diff}$ presents itself as a 10 pF single ended load $C_{left}$). The amplifier has dynamic settling requirements of $\epsilon = 0.025\%$ and $t_s = 125\mu s$, and the static settling requires a DC gain greater than 102 dB over an output voltage swing of $\pm 850mV$.

Figures 11 gives the Spectre simulation results plotting the $\eta_g$ values as a function of the device W/L ratio at $I_d = 1\mu A$, and Figure 12 plots the $\gamma$ values as a function of the $\eta_g$ and channel length. (note: the $\gamma$ values for the P-type MOSFETS were also collected and used for the values in Table 1, however, the values are similar to those from Figure 12 and are not presented here.)

Figure 11. Spectre simulation results sweeping channel $W/L$ ratio with fixed $I_d = 1\mu A$ of the 130nm N and P-type MOSFET.

Using Figures 11 and 12, and the fact that the Figure 2 folded cascode $\frac{I_{d2}}{I_{d1}} = 1$ and $\frac{I_{d3}}{I_{d4}} = 2$, values for $\eta_g$ and $\gamma$...
can be chosen which will allow (7) to be solved to meet the \( nf \leq 0.36 \) requirement. Table 1 lists the noise factor values which are used for this design.

Table 1. Noise Factor \( \gamma \) and \( \eta_{g_m} \) values.

| \( \eta_{g_m1} \) | Fig. 11 | 28 |
| \( \gamma_i \) | Fig. 12 | 0.35 |
| \( \eta_{g_m2,3} \) | Fig. 11 | 14 |
| \( \gamma_{ss} \) | Fig. 12 | 0.6 |
| \( nf \) | (7) | 3.57 |

Solving (1) for the given settling requirements gives (31).

\[
-\ln(0.00025) \times 10pF \cdot \frac{1}{125\mu s} \approx 13.3\mu S
\]  

From (31), (6), and Table 1, the required input device bias current is (32).

\[
I_d = \frac{gm}{\eta_{g_m1}} = \frac{13.3\mu S}{28V^{-1}} \approx 480nA
\]

Table 2 lists the \( \eta_{g_m} \) values which have been chosen for each of the design’s MOSFET devices, the device drain current, and the required W/L ratios as given by Figure 11.

The amplifier is a switched capacitor design performing correlated double sampling for \( \frac{1}{4} \) noise rejection. The switching period is \( 125\mu s \) for each half cycle, so the switching frequency is (33).

\[
f_s = \frac{1}{2 \times 125\mu s} = 4kHz
\]

The amplifier has a high pass cutoff frequency of (34) [7] for \( \frac{1}{f} \) noise rejection, and a low pass cutoff frequency (35) from the device \( gm \) and \( C_{left} \), and a noise equivalent bandwidth (NEB) (36) [8] which ranges from about 760 Hz to 16.5 kHz.

\[
f_1 = 0.3f_s = 1.2kHz
\]

\[
f_2 = \frac{gm1F}{2\pi C_{left}} \approx 10.5kHz
\]

\[
f_1 < NEB < f_2 \frac{\pi}{2}
\]

Each device is sized to fit the \( \frac{W}{L} \) ratios in Table 2. Starting with a \( 1\mu m \) channel length, the input and load devices’ \( LW \) gate channel areas are scaled with constant \( W/L \) until their \( \frac{1}{f} \) thermal noise corner frequencies, as determined though Spectre AC noise analysis, are lower than the NEB lower frequency (34).

7 Simulation Results

The amplifier has been designed to meet the settling time and bandwidth requirements set forth by the medical implant. The schematics are assembled using Cadence Design Framework II, and Spectre simulations are used to verify its small and large signal performance. The gain boosted folded cascode amplifier is simulated using the test schematic from Figure 13, which has an effective differential output impedance of 5 pF, and a feedback factor of \( \frac{1}{20} \).
AC simulations show that the amplifier has an open loop DC gain of a little more than 150 dB, and the closed loop 3 dB cut off frequency is a little bit more than 10 kHz as calculated by (35).

Figure 15 gives the open loop DC gain over the amplifier’s output voltage range. The plot shows that over the required ±850mV output voltage swing, the amplifier can deliver > 114dB of open loop DC gain.

Figure 16 shows the step response of the amplifier under load and no load conditions. Considering stability, there is no ringing present in the non loaded response. In regards to the accuracy and settling time, the step response verifies that the amplifier settles to the required output voltage in the 125µs of time which it is given to settle.

Noise and power simulations were also performed. The total DC current consumed by the gain boosted folded cascode system, including the bias reference generator and the gain boosting amplifiers, is a little less than 2.5µA. An AC noise simulation performed on the circuit from Figure 13 shows the total input referred noise integrated over the amplifier’s effective noise bandwidth (36) is $V_{in,noise} \approx 653nV$.

The $SNR_{db}$ of the amplifier in its feedback configuration is (37), and the effective number of bits from the

$$SNR_{db} = 10 \log_{10} \frac{V_{out, rms}^2}{kT \frac{C_{eff}}{C_{par}}}$$

$$ENOBO = \frac{SNR_{db} - 1.76}{6.02}$$

$$ENOBO \approx 11.1\text{bits}$$
8 Conclusion

A gain boosted cascode amplifier has been designed to meet the speed, accuracy, and low power needs of a wireless medical implant. The folded cascode amplifier structure was sized to meet the settling and noise factor requirements, and transistors were sized according to their transconductance efficiency. A gain boosting network has been implemented using telescopic cascode amplifiers because of their greater gain and lower power requirements when compared to a folded cascode architecture, and a method for level shifting their input voltages has been presented. The gain boosters were designed to meet the stability requirements of the folded cascode amplifier, and a noise analysis of the gain boosted network has been performed. The amplifier was implemented in Cadence Design Framework II, and put through AC, DC, Transient, and noise simulations to verify its performance. The amplifier meets the design requirements set forth by the implant’s signal conditioning circuitry, and does so consuming a minimum of power consumption.

References


