SIMULATION AND EVALUATION OF HERIC AND H5 TRANSFORMERLESS INVERTER TOPOLOGIES

Muh’d I. Alzoubi, Amanullah Maung Than Oo, Salahuddin Azad
Central Queensland University
Bruce Highway, North Rockhampton 4702, Australia
m.alzoubi@cqu.edu.au

ABSTRACT
Most of the inverters have an isolation transformer which prevents or limits fault current between AC and DC circuits under most fault conditions. If the transformer is excluded from the system, it would increase the PV system efficiency and decrease the size of its installations, which will lead to a lower cost for the whole investment. Thus, elimination of the transformer has to be considered carefully because a galvanic connection appears between the PV arrays and the ground in the absence of an isolation transformer. The galvanic connection causes the stray capacitance between the PV arrays structure and the ground to produce a leakage current. In this paper, a review of full bridge topology with bipolar and unipolar scheme and half bridge topology carried out in regard leakage current. In addition, HERIC and H5 topologies are simulated and leakage current in these topologies are evaluated.

KEY WORDS
Transformerless inverter, leakage current, simulation, HERIC, H5 full bridge modulation.

1. Introduction

There are some safety concerns in regards to the transformerless inverters, e.g., current leakages. The absence of galvanic separation in this kind of inverters leads to higher residual currents, which is dependent upon the inverter configuration. It is feared that the DC-side faults in transformerless inverters could probably be conducted directly to the AC grid leading to grave tribulations within the public grid. This is contrary to inverters which have transformers which have almost negligible leakages currents [1] [2]. Analysis of the transformerless PV inverter topologies in terms of leakage current is very important for the safety of the individuals. Furthermore, development of guiding principles that will ensure reduced leakage current and thus more protection for the human being [3] [4].

The most common transformerless inverter topology is H-bridge topology consisting of a H-bridge with bipolar, unipolar or, hybrid modulation, HERIC and H5. These topologies lack galvanic isolation between PV array and the grid. When the PV system is directly connected to the power grid, a direct leakage current may be created because of the variations of the potential between the grid and PV array. The variation in voltage charges and discharges the parasitic capacitance created between the Photovoltaic’s surface and the earthed frame. This is depicted in Figure 1 below. The resonant circuit is formed through the connection of both the parasitic capacitance and DC lines linking the Photovoltaic to the inverter. The frequency of the resonant depends on the size of the photovoltaic array and DC cable length effects [5] [6] [2].

![Figure 1. Parasitic capacitance between PV and ground](image-url)

PV module costs are becoming affordable; this is as a result of the reduced manufacturing costs which excludes isolation transformers. Topologies employing a high frequency transformer in the DC-DC converter have experienced a reduction in efficiency due to leakage in the transformer. A transformerless solution offers the aforementioned advantages. However, there are some safety issues arising from transformerless systems because of the PV panel parasitic capacitance [1] [7] [8]. Leakage currents are generated particularly when there is variation in voltage across the stray capacitance. Various levels of current leakages survive in real PV systems. Current leakages are consequently allowed up to a certain limits, which are less hazardous [9] [10]. Empirically, a typical capacitance value ranging from 50-150 nF/kW was determined in the past between the solar array and ground. This value is getting smaller with the improved technologies in manufacturing the PV system. This is dependent upon the prevailing weather conditions and the configuration of the system. As a result, this leads to leakage currents between the PV panel and ground,
depending on the topology of the inverter. The extent by which the current leaks is principally determined by the voltage’s ebb and flow, rate of recurrence, amplitude and parasitic capacitance present at the PV panel’s terminals [11] [12] [13].

Some studies reveal that the surface of a PV array is an electric hazard when an individual comes into contact with it. Basing on various transformerless inverter topologies when an individual has direct contact with the exterior part of the panel the probability of ground current flowing through the individual is high depending on the level of the current hence resultant shock or injury.

2. Common Mode Voltage

When transformer is excluded from the inverter in the in the grid connected PV system a galvanic connection appears between the PV arrays and the distributed grid leading to produce a common mode voltage, the impact of the common mode voltage on the whole PV system is highly dependent on the transformerless inverter topology used to convert DC voltage to AC voltage. Thus, the ground leakage current generated from the common mode voltage may generate more losses in PV system and then reducing the efficiency and may produce more electromagnetic interference (EMI) and increase the distortion of the grid current. Fire hazard is another issue that may happen due to the leakage currents. The leakage current can flow through the parts and components to heat and cause fire and may affect the equipment’s in the system [14] [4] [1]. Moreover, leakage currents may accelerate the degradation process of the PV arrays. In addition, human can be exposed to electrical shock leading to serious injury. Therefore, in this situation its preferred to use transformerless inverter topology that have minimum leakage current or the one that have no varying common mode voltage such as HERIC or H5 topology which have a constant common mode voltage [15] [16].

The common mode voltage value can be calculated from this equation:

\[ V_{COMM} = \frac{V_A+V_B}{2}, \frac{(V_A-V_B)(L_2-L_1)}{(2(L_1+L_2))} \]

For single phase transformerless inverter topology with the inductors \( L_1 = L_2 \)

\[ V_{COMM} = \frac{V_A+V_B}{2} \]

Different types of topologies are used in single phase transformerless inverter in PV systems. The most common inverter topology is the H-bridge or full bridge topology. HERIC and H5 topology are derived from the full bridge and consist the fundamental of the H-bridge with extra switches.

2.1 Full Bridge Bipolar Modulation Scheme

Full bridge bipolar modulation is made up of four switches, In the case of this modulation the switches are switched in diagonal, S1 synchronous with S4 and S3 with S2. Thus AC voltage can be generated, resulting in a constant common-mode voltage with only two level output voltage (\( +V_{DC} \) and \( -V_{DC} \)) with no possible to generate zero output voltage, and the voltage to ground of the PV array will only fluctuate with the grid frequency with an amplitude half of the peak value of the grid voltage [17] [13] [18]. The different combination of the switching state as show in table 1. The main advantages of this converter is that \( V_{g-pv} \) has only a grid frequency components and no switching frequency components, leading a very low leakage current and low electromagnetic interface (EMI).

The disadvantages of this topology are the generated output voltage vary from (\( +V_{DC} \) to \( -V_{DC} \) to \( +V_{DC} \)) resulting in high core losses, and the switching ripple in the current equals the switching frequency as shown in figure 2 & 3, which mean higher filtering requirements. The efficiency of this type of modulation is up to 96.5 %, which is low due to the reactive power exchange between the two inductors \( L_{1,2} \) and the capacitance \( C_{PV} \) during freewheeling and high core losses in the output filter, due to the fact that two switches are simultaneously switched every switching period [1] [6] [19]. Figure 2 shows the switching state of the bipolar FB modulation and table one shows the two combinations of the switching state.

<table>
<thead>
<tr>
<th>Switching state</th>
<th>Switches (S) ON</th>
<th>Switches (S) OFF</th>
<th>V_{OUT}</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>S1, S4</td>
<td>S2, S3</td>
<td>+V_{DC}</td>
</tr>
<tr>
<td>B</td>
<td>S2, S3</td>
<td>S1, S4</td>
<td>-V_{DC}</td>
</tr>
</tbody>
</table>

Table 1: Switching state of bipolar modulation scheme

![Figure 2: switching state of bipolar FB modulation](image)
2.2 Full Bridge Unipolar Modulation Scheme

A full bridge converter which uses unipolar switching is called a three level converter. A unipolar modulation switching scheme is where the output of the converter (V_{OUT}) switches or varies between +V_{DC} and zero during the positive half wave and between -V_{DC} and zero during the negative half wave. Unlike bipolar switching, unipolar switching requires at least three different switching states as the junction voltage (V_{OUT}) can be either +V_{DC}, -V_{DC} or zero although most inverters implement four switching states by having a different switching combination to create the zero junction voltage for each half wave as shown in table 2 which shows some of the different combination of switching state [20] [4]. In the positive half cycle, S_{4} is conducting while S_{1}-S_{2} commutates at the switching frequency. However, in the negative half cycle, S_{2} is conducting at the same time as pair S_{1}-S_{4} commutates at the switching frequency. figure 4 and 5 show the switching state of the positive half cycle of the unipolar modulation, while figure 6 and 7 shows the negative cycle of this modulation scheme.

<table>
<thead>
<tr>
<th>Switching state</th>
<th>Switches (S) ON</th>
<th>Switches (S) OFF</th>
<th>V_{OUT}</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>S1, S4</td>
<td>S2, S3</td>
<td>+V_{DC}</td>
</tr>
<tr>
<td>B</td>
<td>S2, S4</td>
<td>S1, S3</td>
<td>0</td>
</tr>
<tr>
<td>C</td>
<td>S2, S3</td>
<td>S1, S4</td>
<td>-V_{DC}</td>
</tr>
<tr>
<td>D</td>
<td>S2, S4</td>
<td>S1, S3</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 2: the switching state of unipolar modulation scheme

The efficiency of this modulation is up to 98% due to reduced losses during zero voltage states. In addition, the switching ripple in the current twice the switching frequency, leading to lower filtering requirements [10] [2]. The disadvantage of this topology is that the Vg-vp has switching frequency components leading high leakage current and EMI. This high leakage current makes the FB-
unipolar unsafe. Figure 3 and table 2 shows the different switching state in FB unipolar modulation.

2.3 Full Bridge With Hybrid Modulation Scheme

In this type of modulation, one leg is switched at grid frequency and the other leg at high frequency. Thus AC current can be generated and the output Voltage across the filter is unipolar and vary from zero to +Vdc to zero to -Vdc, resulting lower core losses. The efficiency is up to 98 % because there is no reactive power exchange between $L_{1,2}$ and $C_{PV}$ during zero voltage and to lower frequency switching in one leg [13].

The disadvantages of this topology are this modulation only works for a two quadrant operation, and the switching ripple in the current equals switching frequency required a higher filtering. In addition the $V_{g-pv}$ has square wave variation at grid frequency, leading to high leakage current peaks and large EMI filtering requirements. Figure 8 & 9 show the switching states in FB with hybrid modulation scheme [21] [22].

2.4 H-Bridge with AC Bypass (HERIC)

The H-Bridge with AC bypass also known as another topology that is derived from the highly efficient and reliable inverter concept (HERIC) bypasses the AC side by addition of of a bypass leg using two back-to-back insulated gate bipolar transistors (IGBTs). The modification includes two extra switches (S5-S6) each connected in series with a diode. During the zero voltage vector, depending on the sign of the reference voltage, either S5 or S6 are turned ON, while S1, S2, S3 and S4 are all in their OFF state and the PV array is disconnected from the grid. This way there is a possibility of achieving the zero voltage vectors and the output voltage will be unipolar, having the same frequency as the switching frequency and there will be no high frequency fluctuations present at the DC terminals of the PV array as shown in table 3.

Some types of it combine the advantages for the three-level output voltage of the unipolar modulation with the reduced common-mode voltage. This has implications on
the efficiency of the inverter which increases without any compromises on the common-mode behaviour of the whole system. Some of the main features of this topology is its ability to prevent the exchange of reactive power between $L_{(1,2)}$ and the $C_{PV}$ during the zero voltage state which ultimately increases in the efficiency of the system. Also, it allows the isolation of the PV module from the grid during the zero voltage state which then eliminates the high-frequency content of the $V_{g-pv}$ [1] [21] [23]. The main advantage of the topology is the unipolar voltage across the filter which results in lower core losses. Also, it has very high efficiency because of the lack of reactive power mentioned above. Lastly, it has only a grid frequency component which yields very low leakage current and EMI also due to lack of switching frequency components [15] [10]. Figure 10 &11 show the positive cycle while figure 12 & 13 show the negative cycle of HERIC topology.

<table>
<thead>
<tr>
<th>Switching state</th>
<th>Switches (S)</th>
<th>Switches (S)</th>
<th>( V_{OUT} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>S1, S4, S6</td>
<td>S2, S3, S5</td>
<td>(+V_{DC})</td>
</tr>
<tr>
<td>B</td>
<td>S6</td>
<td>S1, S2, S3, S4, S5</td>
<td>0</td>
</tr>
<tr>
<td>C</td>
<td>S2, S3, S5</td>
<td>S1, S4, S6</td>
<td>(-V_{DC})</td>
</tr>
<tr>
<td>D</td>
<td>S5</td>
<td>S1, S2, S3, S4, S6</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 3: switching state of HERIC topology

![Figure 10: switching state of HERIC modulation (A)](image)

![Figure 11: switching state of HERIC modulation (B)](image)

![Figure 12: switching state of HERIC modulation (C)](image)

![Figure 13: switching state of HERIC modulation (D)](image)
For simulation results using Matlab (simpower) with the following parameters, filter inductance $L_{(1,2)} = 1.8$ mH; input voltage $V_{dc} = 350$ V; dc link capacitance $C_{pv} = 250 \mu F$ with 8kHz switching frequency. Figure 14 shows the simulation result of the load current of the HERIC topology while figure 15 shows the leakage current in this topology with constant common mode voltage and very small leakage current less than 20mA.

![Figure 14: load current in HERIC topology](image)

![Figure 15: leakage current in HERIC topology](image)

### 2.5 H-Bridge with dc Bypass (H5)

This topology has an added transistor which is the basis for its name and was patented by SMA in 2005; the concept of this topology is to generate the zero voltage and so getting three output voltages. The operation of this topology is S1 and S3 are switched with the grid frequency; S1 is continuously ON during the positive half, while S3 is continuously ON during the negative half of the reference voltage. To make the positive voltage vector, S5 and S4 are switched simultaneously with high frequency, while S1 is ON and the current will flow through S5- S1 returning through S4, during the zero voltage vector, S5 and S4 are turned OFF and the freewheeling current finds its path through S1- S3. The negative voltage vector is done by switching S5 and S2 simultaneously with high frequency, while S3 is ON, during the corresponding half period of the reference voltage and the current will flow through S5- S3 returning through S2 the PV panels are disconnected from the grid during the current freewheeling periods resulting to an almost constant common mode voltage [23] [1] [13] [24].

Table 4 shows the switching state of the H5 topology, figure16,17,18 and 19 which show the three level output with both positive and negative cycle. The layout of the topology prevents the exchange of reactive powers between the $L_1$ and the $C_{pv}$ during zero voltage state which then increases the efficiency of the system. It also allows the prevention of contact between the PV module from the grid during the zero voltage state which then eliminates the high-frequency content of the $V_{g-pv}$ [12] [25].

<table>
<thead>
<tr>
<th>Switching state</th>
<th>Switches (S) ON</th>
<th>Switches (S) OFF</th>
<th>$V_{OUT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>S1, S4, S5</td>
<td>S2, S3</td>
<td>$+V_{DC}$</td>
</tr>
<tr>
<td>B</td>
<td>S1</td>
<td>S2, S3, S4, S5</td>
<td>0</td>
</tr>
<tr>
<td>C</td>
<td>S2, S3, S5</td>
<td>S1, S4</td>
<td>$-V_{DC}$</td>
</tr>
<tr>
<td>D</td>
<td>S3</td>
<td>S1, S2, S4, S5</td>
<td>0</td>
</tr>
</tbody>
</table>

**Table 4: the switching state of H5 topology**

Some of the advantages of the H5 topology are its ability to be unipolar resulting then to the lower core losses. There is also high efficiency, amounting to 98%, because of the lack of power exchange between the $L_1$ and the $C_{pv}$ during zero voltage and to the lower frequency switching in one leg. However, because of the added transistor, there is also an additional extra switch. Also, there are three switches that are conducting during active vector which then results to the higher conduction losses but without the overall efficiency being affected[1] [10].

---

Table 2: Component parameter values

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{(1,2)}$</td>
<td>1.8 mH</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>350 V</td>
</tr>
<tr>
<td>$C_{pv}$</td>
<td>250 $\mu F$</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>8kHz</td>
</tr>
</tbody>
</table>

---

217
The simulation results using Matlab (simpower) for H5 topology with the same parameters used in HERIC topology can be shown in figure 20 which show the load current in H5, while figure 21 show the leakage current which under 20 mA and close to zero.
3. Conclusion

H5 and HERIC topologies have a three-level output voltage. This increases the efficiency as both the switches and the output inductor are subject to half of the input voltage stress. The zero voltage state is achieved by shorting the grid using the higher switches of the H bridge (H5) with one switch in the DC side or by use two switches in series (back to back) in the AC side as in (HERIC). H5 and HERIC isolate the PV panels from the grid during zero voltage. The main features of these topologies are their ability to prevent the exchange of reactive power between the inductors \( L (1,2) \) and the capacitance \( C_p \) during the zero voltage state which ultimately increases in the efficiency of the system. Both of HERIC and H5 are simulated in regard the leakage current and both topologies showed that they have very low leakage current close to zero leading to high efficiency for the PV system.

References


