D-TDMA DATA BUSES WITH CSMA/CD ARBITRATION BUS ON WIRELESS 3D IC

ABSTRACT
Because of the increase in cost for chip fabrication, designing a chip family in accordance with the application is becoming an expensive choice. Wireless 3D IC design offers flexibility to connect known-good-dies selected after chip fabrication. It can stack an arbitrary number of chips at low cost. In this paper, dynamic time division multiple access (D-TDMA) is used for vertical broadcast buses for high communication efficiency of interchip network. However, to implement simple D-TDMA based 3D IC, large area and energy overheads are needed for arbitration since another inductor is needed for sending just several bits as arbitration signal in addition to an inductor for the data transfer. We resolve this problem to employ a carrier sense multiple access with collision detection (CSMA/CD) for arbitration of D-TDMA vertical broadcast buses. Evaluation results show that the proposed bus architecture reduces the number of inductors by 73.6% compared to a simple counterpart which employs D-TDMA based 3D buses. The results also show that an application execution time increases only by 0.3% at most.

KEY WORDS
Network-on-Chip, Chip Multi-Processor, Wireless 3D IC, Bus

1 Introduction
With advances in semiconductor technology, low-cost design is one of important factors in chip fabrication. 3D IC design could be constituted by selecting known-good-dies and an arbitrary number of chips can be stacked at a low cost. To design 3D ICs, various interconnection techniques have been developed, e.g., wire-bonding, microbump, Through-silicon via (TSV), and wireless interconnect (i.e., capacitive-coupling and inductive-coupling) between stacked dies [1][2][3][4].

TSVs or microbumps are often used for vertical interconnection in 3D IC design by reason of performance [5]. On the other hand, wireless 3D IC design that uses inductive-coupling has a high flexibility to connect known-good-dies selected after chip fabrication. This advantage of wireless 3D IC enables us greatly reduce the cost for the design of a chip family in accordance with a target application. In this paper, therefore, we focus on inductive-coupling wireless 3D ICs.

In the wireless 3D ICs, a magnetic field generated between a pair of transmitter and receiver coils (i.e., inductors) enables interchip communication. Since a magnetic field can go through multiple chips by expanding an area of inductor, vertical links can be formed in two ways. Wireless Point-to-point links are used for communication between only two neighbor chips. Wireless buses can be used for communication between multiple chips at the same two-dimensional coordinates in more than two chips. In these buses, even if data are sent from the uppermost chip to the bottommost chip, the data transfer to any chips takes one-hop distance. However, the chip can send data only if the other chips do not use the vertical bus. Thus, chips often cannot efficiently use the bandwidth of vertical buses.

A vertical bus can be formed with various ways. Dynamic time division multiple access (D-TDMA), in which a dynamically arbitrated chip can access the bus, is efficient in terms of bandwidth. In wireless 3D IC, however, D-TDMA is not a cost-efficient vertical bus access control mechanism if we implement it in a naive manner, because implementing control signals is expensive. Even if a 1-bit control signal is needed to be sent in wireless 3D IC, an inductor of the same size as that for sending data is needed. Note that a single inductor provides an 8-Gb/s throughput, while it consumes a 225-μm × 225-μm area [6]. Obviously, implementing such control signals is waste of bandwidth.

To cope with this problem, in this paper, we propose a wireless hybrid bus 3D IC architecture. We introduce one carrier sense multiple access with collision detection (CSMA/CD) for vertical broadcast bus for arbitration of D-TDMA buses. This architecture enables us to reduce the number of inductors and to implement D-TDMA buses for
vertical interconnection with a low cost.

The rest of this paper is organized as follows. Section 2 surveys inductive-coupling technology and bus-based ICs. Section 3 proposes a hybrid wireless 3D bus architecture in order to reduce area and power overheads by implementing control signals for D-TDMA arbitration. Section 4 evaluates proposed architecture. Section 5 concludes this paper.

2 Wireless 3D Bus Architecture

2.1 2D and 3D Chip-MultiProcessor (CMP)

We assume to implement Chip-MultiProcessor (CMP) using wireless 3D buses. First, we describe 2D CMPs which are a part of the 3D CMPs.

Fig 1 shows an example of 2D CMP. In Fig 1, 16 tiles are implemented on a single chip. Each tile consists of a processing core or L2 cache bank. An on-chip router is implemented on each tile. That is, Fig 1 consists of 8 processing cores and 8 L2 caches. Each tile has an on-chip router. Note that main memory module and memory controller are connected at corners of a chip.

In Fig 1, tiles communicate with each other via on-chip routers. All L2 cache banks are shared by all processing cores. Static Non-Uniform Cache Access (SNUCA) is selected as a cache architecture [7]. We assume that cache coherence is guaranteed.

A 3D CMP can be formed by stacking 2D CMPs. Fig 2 is an example of 3D CMP, which is constituted of 2D CMPs shown in Fig 1. Four chips are vertically stacked in a package. 3DIC enables us to stack multiple chips, each of which consists of different process technology, logic, and DRAM in a single package. By fabricating various types of chips in a single package, wire length and pin count can be reduced and performance can be improved.

2.2 Characteristics of Inductive-Coupling Interchip Links

In 3D CMPs, interchip communication is an important factor for performance and cost. In previous studies, microbumps or TSVs are often used for vertical links [8]. In this paper, we select wireless chip interconnection: capacitive-coupling and inductive-coupling. Because capacitive-coupling is used for face-to-face communication with two chips, we adopt inductive-coupling which has a great potential for the flexibility for customizing chips by communicating each chip wirelessly.

Potential for the flexibility means there would be a possibility that we can add or remove chips after fabrication and easily customize of system-in-package because of wireless interchip connection in the future [1]. The flexibility also enables us to improve application performance which may be restricted by computational performance or memory bandwidth. If the performance is restricted by the former factor, we can deal with this problem by stacking more processor chips. If it is restricted by the latter factor, we can improve performance by stacking cache chip.

As shown in Fig 3, inductive-coupling is an interconnection technique between stacked dies. To communicate with each other, square or hexagonal coil is formed on metal layers of a chip and used as serial data transceiver, as shown in Fig 4. Because a coil can be formed from two arbitrary metal layers of a chip, special fabrication technology is not needed. Coils implemented on different chips generate a magnetic field. Since a magnetic field can go through multiple chips, data multicast can be achieved if inductors are superimposed on each other.

Size of a coil is selected according to communication distance (i.e., the number of chips and chip thickness). For example, 100\(\mu\)m\(\times\)100\(\mu\)m coils are used in a four-chip stack in which chip thickness is 10\(\mu\)m [9]. In [6], in order to provide 8 Gb/s per an inductor, a coil size is 225\(\mu\)m\(\times\)225\(\mu\)m for four-chip stack. In this case, chip thickness is 30\(\mu\)m.

Inductive-coupling has various advantages over the other techniques. Inductive-coupling vertical link has a contact-less interface without ESD protection device, and provides more than 1GHz with a low energy dissipation (0.14pJ per bit) and a low bit-error rate (BER < 10\(^{-12}\)). In particular, one of the biggest advantages of inductive-coupling is that only two arbitrary metal layers are needed for coils, and thus the remaining transistors are available for memory or random logic, while TSVs consume all of them. In addition, since there is a possibility that an on-chip router can be implemented under coils, we can reduce required area in an inductive-coupling vertical link. While TSV-based vertical link consumes area for a router in addition to TSVs, an inductive-coupling vertical link requires area for a router or coils, whichever is larger. With tech-
nique of microbump, we can implement vertical links similarly to inductive-coupling links and reduce area. However, at most two chips can be stacked because of stacking chips only face-to-face manner by using microbump. In inductive-coupling wireless vertical links, more than two chips can be stacked.

In the case of vertical link of inductive-coupling, we can implement nine inductors (i.e., a single clock inductor and eight data inductors) and an on-chip router in the same area which consumes $675 \mu m \times 675 \mu m$. In contrast, in the case of TSV-based vertical link, we can implement an on-chip router which consumes $500 \mu m \times 800 \mu m$, which we estimates from [10], and 329 TSVs in the remaining area. As a result, throughput of a TSV-based vertical link and an inductive-coupling vertical link are 64 Gb/s and 65.8 Gb/s respectively per a vertical link [6]. In this case, an inductive-coupling vertical link is almost comparable with a TSV-based vertical link in terms of throughput per area.

Inductive-coupling has scalability to stack more than two chips and flexibility for customizing the number of arbitrary chips after chip fabrication. Inductive-coupling is already used for various purposes in fields of multiprocessor and reconfigurable device [11]. However, in order to transfer serial data at high bit rate, high-speed transmit inductor is needed and energy consumption is increased.

### 2.3 Various Vertical Link Architecture

In a wireless 3D IC, a communication distance can be increased by increasing the size of a coil. For that reason, there are two ways to form a vertical link in wireless 3D IC. Point-to-point (P2P) method is used for communication between only two neighbor chips. Bus method enables to broadcast data to all chips. With the former method, a inductor approximately consumes about $30 \mu m \times 30 \mu m \sim 150 \mu m \times 150 \mu m$ area. In contrast, with the latter method, it consumes about $250 \mu m \times 250 \mu m \sim 350 \mu m \times 350 \mu m$ area. Note that the required area varies depending on chip thickness.

In 3D ICs, an interchips distance is much shorter than an intrachip distance between adjacent routers. In order to take advantage of this benefit, bus method has been selected as vertical link in previous studies [12][8]. In addition, bus method can be used to communicate from the uppermost chip to the bottommost chip by one hop. Compared to P2P, bus method has an advantage that average hop count is reduced.

However, in order to use the bus method, bus controllers are needed. Because there is a possibility that multiple source nodes transmit data to a vertical bus at the same time. Moreover, the bus method has another problem. If one source node already uses a vertical bus, the other source nodes need to wait until the first one completes. This problem introduces a performance degradation. We need to cope with this problem by introducing a dynamic bus arbitration.

### 2.4 Bus Access Control Mechanism

In wireless 3D IC, bus access control mechanism can be considered in three classes: Static time division multiple access (S-TDMA), CSMA/CD, and D-TDMA. TDMA is a common technique that controls a bus access by allocating a communication time-slot to source nodes.

- **S-TDMA**
  A time-slot is statically assigned to each chip. Chips can send data only when the time-slot is allocated.

- **CSMA/CD**
  Chips can send data in an arbitrary timing. If chips send data to a bus at the same time, conflicting chips are required to wait a random time and then retransmit the data.

- **D-TDMA**
  Chips can send data when they win the arbitration. A centralized arbiter dynamically allocates a bus grant to one of requesting chips.

Although it is easy to implement S-TDMA for vertical buses because no additional control lines (i.e., dedicated inductors) are needed, it is not efficient since a time-slot is assigned to chips that do not have data to be sent. CSMA/CD method is more efficient than S-TDMA method because data can be sent in a arbitrary timing. However, a collision detection mechanism and retransmission strategy are needed for inductive-coupling buses.

D-TDMA is also efficient, because a bus mastership is efficiently distributed by a centralized arbiter. In order to form a D-TDMA bus, additional control signals are needed for all the chips to send a bus request to the arbiter. Since performance of D-TDMA is high, considering the overhead of adding a bus arbiter, D-TDMA is generally used for vertical bus access control mechanism in 3D IC. We also try to use D-TDMA in wireless 3D IC. However, there is a specific problem which is introduced when D-TDMA buses are used for inductive-coupling.

### 2.5 Specific Problem of Implementing D-TDMA Buses in Wireless 3D IC

A vertical bus in wireless 3D IC can be implemented by using inductive-coupling. Because of wireless communication between chips, we need to take into account a specific problem described below. Previous study [13] in which D-TDMA bus is used for vertical link is based on TSV for forming vertical bus. That is, vertical links based on TSV are classified as a wired connection. With wired vertical connection, it is easy to add several-bit control signals needed for bus arbitration.

In contrast, with wireless vertical connection, it is costly to add such control signals because of large area and energy overheads. In wireless 3D IC, coils for control signals are the same size as coils for sending data. Obviously, implementing such control signals is waste of bandwidth.

To cope with this problem, in previous work [14] S-TDMA is adopted as vertical bus access control mechanism. Since S-TDMA is inferior to the other bus access control mechanism in performance, [14] proposes architecture for inductive-coupling through chip interfaces to improve performance. By comparison, we use D-TDMA bus as vertical bus in an effort to reduce additional control lines.
3 Hybrid Wireless 3D Bus Architecture

3.1 Outline of Our Proposed Architecture

It is costly to implement a D-TDMA bus in wireless 3D IC in a naive manner since area and energy overheads increase by additional inductors for control lines. In this section, we propose a hybrid wireless 3D bus architecture that tries to reduce additional control lines by introducing an additional CSMA/CD bus for arbitration.

In [6], CSMA/CD bus based wireless 3D bus architecture has been proposed. Its feasibility has been demonstrated in [6]. Also inductor design for CSMA/CD has been discussed in [6]. We simply employ the CSMA/CD inductor design introduced in [6].

Fig 5 shows overview of our proposed architecture. In this example, the system consists of four chips which are drawn in light blue; D-TDMA buses which are drawn as yellow vertical lines; CSMA/CD bus which is drawn as a red vertical line at the center of the chips; nodes and bus arbiters which are drawn as white and blue rectangle respectively. A node indicates a processor core or L2 cache. Bus arbiter is in charge of the bus arbitration for D-TDMA.

Each chip has an identical structure to the tile shown in Fig 1. That is, one chip has 16 nodes. Since each node is connected to one D-TDMA bus and it needs a bus arbiter, 16 D-TDMA buses and 16 bus arbiter are needed in total. Note that a bus arbiter can be implemented at an arbitrary chip. In this paper, we place it in the uppermost chip.

Nodes are connected each other via on-chip routers in chips, each of which has a $4 \times 4$ mesh topology. Packets are transferred via on-chip routers. In contrast, control signals for bus arbitration are connected via a crossbar interconnect. That is, each node and CSMA/CD bus are connected by one hop. Only control signals are transferred via a crossbar interconnect.

Fig 6 emphasizes the bottommost chip and CSMA/CD bus in the proposed architecture. In Fig 6, a green line indicates a crossbar interconnect. Using this crossbar, control signals can be sent to a CSMA/CD arbitration bus by one hop.

We propose this architecture to send data via D-TDMA buses and reduce additional inductors at the same time. Additional CSMA/CD bus at the center of the chips is a key component in our proposal. In the proposed architecture, all control signals for D-TDMA bus arbitration go through the CSMA/CD bus. Thus, there is no need for additional control lines along D-TDMA bus and additional inductors.

3.2 Behavior of Proposed Architecture

In this subsection, we explain a processing flow in the proposed architecture by using a simple example that sends a data packet. We assume that data packets are sent from the lower left node (Src) to the upper right node (Dst) in Fig 5. Here we introduce an Arbitration flit that contains the source node ID and packet length of sending data. An Arbitration flit consists of a set of several-bit control signals. Arbitration flits precede data packets via a CSMA/CD bus and perform D-TDMA bus arbitration for data packets in advance. As a result, data packets can use D-TDMA bus without additional control signals. Also we introduce Grant flit that notifies a bus mastership to one of requesting chips. After Grant flit is broadcasted, the grant chip can use the vertical bus without any collisions.

**STEP I** Arbitration flit is sent from source node (Src) to CSMA/CD bus via a crossbar shown in Fig 6. Note that Arbitration flit is transmitted by one hop to CSMA/CD bus using the crossbar interconnect. If an inductor at the source node is turned off, power-on operation is performed.

**STEP II** Arbitration flit moves upward along a CSMA/CD bus. At this step, Arbitration flit is split into two parts. One goes to the chip which is located at destination node (Dst) and the other goes to the chip in which bus arbiter is placed, i.e., the uppermost chip in Fig 6. The former reaches the bus arbiter and then the bus arbiter executes a D-TDMA bus arbitration based on information of Arbitration flit. The latter reaches the receiver node which is connected to source node via D-TDMA bus, i.e., the leftmost node in the second chip from the top in Fig 7. If an inductor is turned off, power-on operation is performed.

![Figure 5. Overview of Hybrid bus wireless 3D IC](image1)

![Figure 6. Network for control signals](image2)
STEP III Bus arbiter broadcasts the result of bus arbitration as Grant flit via the D-TDMA bus.

STEP IV Based on the bus arbitration result, the source node starts sending data packet.

The above steps correspond to STEPs I to IV in Fig 7. STEP I and II are shown in green lines, STEP III is shown in a blue line, and STEP IV is shown in a yellow line. To perform these steps, we select an elevator-first routing on which packets move in the z-axis direction with priority.

Until sending data packets, the above steps need to be executed. For that reason, an average packet arrival time may be delayed compared with a naive 3D bus architecture. However, we expect the delay is not large enough to move Arbitration flit to an arbitration bus (CSMA/CD bus) in one hop. In Section 4, we evaluate the performance degradation caused by this delay.

This policy enables us to use vertical D-TDMA buses in wireless 3D IC and to reduce additional inductors at the same time. Reducing additional inductors can reduce area and energy overheads, and in addition, it can further reduce the energy by turning off inductors until sending data packets.

As it was previously mentioned at STEPs I and II, Arbitration flits can turn on inductors that have traversed if they are turned off. In addition, Arbitration flits always precede data packets. Therefore, inductors of D-TDMA buses can be turned off until data packets come. As a result, energy consumption is further reduced. In Section 4.3.4, we evaluate benefits when turning on/off the inductors.

3.3 On-chip Router Design

Fig 8 shows our on-chip router design. In this router, packets are transferred in the order from left to right. A router consists of various components: input channels, route computation units, an arbiter, a crossbar, output channels, and a bus controller for implementing our proposed architecture, respectively from left to right in Fig 8. In this paper, the number of input/output channels is 6 because data can be received from or sent to north, east, south, west, vertical bus, and local core.

As shown in Fig 8, the bus controller is implemented as part of an output channel which is connected to a vertical bus. Bus controller is in charge of sending Arbitration flit and granting a permission to an output channel for sending data to a vertical bus. In Fig 8 Arbitration flit is transferred along with a green line, and Grant flit is transferred along with a blue line.

For example, a bus request is generated from a source node, Arbitration flit is sent toward CSMA/CD bus along with a green line. After that, using network for control signals shown in Fig 6, Arbitration flit reaches CSMA/CD bus. As described in Section 3.2, using CSMA/CD bus, Arbitration flit reaches the bus arbiter and Grant flit is sent from the bus arbiter to source node. After receiving the Grant flit, bus controller in source node gives a permission to transfer data. In this way data can be sent by using vertical bus.

4 Evaluations

4.1 Evaluation Environment

A basic 2D CMP in this paper consists of L1 I/D cache which is placed in each processor core and all L2 cache banks are shared by all processor cores. We assume that our target 3D CMP consists of 4 chips stacked. Each chip consists of 8 L2 caches and 2 processor cores. Note that, main memory module and memory controller are connected to corners of a chip. All components in the chip, i.e., L2
caches, processor cores, and memory controllers are connected each other by on-chip routers. Interchip communication is done by wireless 3D buses. In this paper, three wireless 3D bus architectures have been introduced so far and we evaluate them in this section.

Table 1 shows parameters of processor and network. In this evaluation, we use the full-system CMP simulator GEMS [15] and NAS Parallel Benchmark [16] as target applications. Note that bandwidth of intrachip link is set as 128-bit and that of interchip link is set as 32-bit. In addition, we implemented the three bus architectures in a hardware descriptive language Verilog HDL and evaluate their area overhead.

4.2 Evaluation Target

In this evaluation, the same chip configuration is assumed for all the chips. We evaluate it by changing only vertical link architecture. For comparisons, three types of architecture is selected: STATIC, DYNAMIC, and PROPOSAL as shown in Fig 9. All vertical links are composed for S-TDMA buses and D-TDMA buses in STATIC and DYNAMIC, respectively. PROPOSAL employs the proposed TDMA buses. In this paper, three wireless 3D bus architectures are introduced: STATIC, DYNAMIC, and PROPOSAL. Therefore, a performance overhead generated by implementing the proposed architecture has a little impact on the whole system.

4.3 Evaluation Results

4.3.1 Execution Time of Applications

Fig 10 shows results of execution time of NAS Parallel Benchmark. From left side of the graph, execution time results of PROPOSAL, DYNAMIC, IDEAL, and STATIC are shown. Note that IDEAL architecture will be explained in Section 4.4. Values in Fig 10 show normalized values in which the result in STATIC is used as a baseline. Fig 10 shows that there is a big difference between results of STATIC and the others. Compared to STATIC, DYNAMIC and PROPOSAL reduce the execution time by 8.8% and 8.5% respectively. The results show that S-TDMA is not effective by contrast with the others. In addition, there is a little difference in execution time between D-TDMA and PROPOSAL. Therefore, a performance overhead generated by implementing the proposed architecture has a little impact on the whole system.

4.3.2 The Number of Inductors

We calculate the number of inductors needed to implement the architecture. \( N \) indicates the number of nodes on a chip and \( k \) is the number of chips. In STATIC, one inductor is needed per one node. Then, \( N \times N \times k \) inductors are needed in total. In DYNAMIC, \( k \) inductors are needed per one node. Then, \( N \times N \times k \times k \) inductors are needed on the whole. Finally, in PROPOSAL, additional inductor is needed to form CSMA/CD bus by contrast with STATIC. On the whole, \( N \times N \times k + k \) inductors are needed.

In the above formula, the number of inductors required can be calculated. Table 2 shows the calculation results of the number of required inductors in target topologies.

Table 2 shows \( k \) times as many inductors as STATIC are required in DYNAMIC. In contrast, additional \( k \) inductors are needed in the proposed architecture. The results show that introducing one CSMA/CD bus significantly reduces the number of required inductors. According to Table 2, PROPOSAL reduces the number of inductors by 73.6% compared to DYNAMIC in \( 4 \times 4 \times 4 \) nodes.

As a result, we can reduce the number of inductors in addition to reducing the area and energy overheads.

4.3.3 Area Overhead

Fig 11 shows area overheads of three types of bus controller after the logic synthesis. From left to right, area overheads of bus controller for implementing PROPOSAL, DYNAMIC, and STATIC reduce the area by 40%, 50%, and 60%, respectively.

Table 2 shows the number of required inductors in target topologies.
DYNAMIC, and STATIC are shown respectively. We implemented bus controllers in a hardware descriptive language Verilog HDL. These RTL models were synthesized with Synopsys Design Compiler based on NANGATE 45-nm process technology. The timing constraint was set to 2000 ps (i.e. 500 MHz).

Fig 11 shows that area overheads of three types of bus controller are almost the same. Area overhead of a bus controller when implementing the proposed architecture is quite small.

### 4.3.4 Ratio of Sleeping Vertical Link

As mentioned in Section 3.2, in PROPOSAL, we can turn off inductors until data packets come. Fig 12 shows the percentage calculated by the active time of the vertical links to a total execution time when IS (integer sort) of NAS Parallel Benchmark is executed. Fig 12 shows that vertical link can be turned off more than 90% of the execution time.

Note that a dynamic energy overhead generated when turning on and off inductors is not considered in this evaluation. However, as it is clear from the results, we can reduce energy consumption by turning off inductors.

In the above evaluations, the proposed architecture is almost the same as STATIC in terms of the number of required inductors. In contrast, the additional area and power overheads are small. In addition, performance of the proposed architecture is almost the same as that of DYNAMIC. Performance overhead is small even when our proposal is implemented.

### 4.4 Number of CSMA/CD Arbitration Buses

In this proposal, the number of CSMA/CD buses is less than that of D-TDMA buses. This means that CSMA/CD bus is possibly become a performance bottleneck. In other words, a number of communication requests to the D-TDMA bus, a number of Arbitration flits are concentrated on CSMA/CD bus and then a number of collisions are happened in the CSMA/CD bus. If Arbitration flits are retransmitted many times, performance will be degraded.

In order to prove that CSMA/CD bus does not become a performance bottleneck, evaluation target IDEAL is added for comparison. IDEAL employs the same architecture as PROPOSAL but it is different from PROPOSAL that any bus collisions do not occur at all in the arbitration CSMA/CD bus. That is, in IDEAL, an ideal condition for PROPOSAL is simulated.

Fig 5 shows that results of the execution time in IDEAL and PROPOSAL are almost the same. This result shows that collisions in CSMA/CD bus rarely happened and the performance overhead is small even if collisions happen. That is, retransmissions at the CSMA/CD bus do not affect the performance significantly and one CSMA/CD bus is enough in this case study. However, CSMA/CD bus may be a bottleneck for applications with a higher utilization of vertical link. To cope with this problem, we can introduce additional CSMA/CD buses. The number of additional CSMA/CD buses required is depending on the number of nodes in a chip and the number of chips. The optimal number of additional CSMA/CD buses will be explored in our future work.
5 Conclusion

In this paper, in order to use D-TDMA buses in the inductive-coupling wireless 3D ICs, we proposed to apply a CSMA/CD arbitration bus to D-TDMA buses in order to reduce the number of inductors. Our new idea is adding a single CSMA/CD bus for arbitration in order to eliminate a lot of arbitration inductors which are needed for D-TDMA bus. In previous studies [6], D-TDMA buses were not used because of implementing control signals is waste of bandwidth. Also we can reduce energy consumption by adopting on/off link schema to our proposed architecture. We can turned off inductors of D-TDMA buses until data packets come. As a result, energy consumption is additionally reduced.

Our proposed architecture has a small overhead in terms of performance, area, and energy. By contrast, compared to 3D ICs with the naive D-TDMA buses, we can reduce 73.6% of the inductors. Compared to S-TDMA bus architecture, we can reduce 8.5% of application execution time on average.

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References


