

JOU, Jer-Min

National Cheng Kung University, Taiwan

Scholarly Contributions [Data Provided by **SCOPUS**]

Jou, J.M., Lee, Y.-L., Wu, S.-S.

[Model-driven design and generation of new multi-facet arbiters: From the design model to the hardware synthesis](#)  
(2011) IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 30 (8), art. no. 5958189, pp. 1184-1196.

Jou, J.-M., Lee, Y.-L.

[An optimal round-robin arbiter design for NoC](#)  
(2010) Journal of Information Science and Engineering, 26 (6), pp. 2047-2058.

Jou, J.M., Wu, S.-S., Lee, Y.-L., Chou, C., Jeang, Y.-L.

[New model-driven design and generation of multi-facet arbiters part I: From the design model to the architecture model](#)  
(2010) Proceedings - Design Automation Conference, pp. 258-261.

Jou, J.M., Lee, Y.-L., Wu, S.-S.

[Efficient design and generation of a multi-facet arbiter](#)  
(2010) Proceedings of the 2010 IEEE 8th Symposium on Application Specific Processors, SASP'10, art. no. 5521137, pp. 111-114.

Lee, Y.-L., Jou, J.M., Chen, Y.-Y.

[A high-speed and decentralized arbiter design for NoC](#)  
(2009) 2009 IEEE/ACS International Conference on Computer Systems and Applications, AICCSA 2009, pp. 350-353.

Lee, Y.-L., Chen, Y.-C., Jou, J.-M., Kuang, S.-R.

[HW/SW co-design of a multi-threaded Java virtual machine](#)  
(2008) International Journal of Electrical Engineering, 15 (2), pp. 109-115.

Jou, J.M., Lee, Y.-L., Lin, C.-Y., Sun, C.-M.

[A novel reconfigurable computation unit for DSP applications](#)  
(2007) Proceedings - IEEE Computer Society Annual Symposium on VLSI: Emerging VLSI Technologies and Architectures, art. no. 4208953, pp. 439-444.

Jou, J.-M., Sun, C.-M., Lin, C.-Y., Lee, Y.-L., Jeang, Y.-L.

[A reconfigurable arithmetic unit array architecture for DSP applications](#)  
(2007) International Journal of Electrical Engineering, 14 (3), pp. 175-183.

Hsu, S.-H., Lin, Y.-X., Jou, J.-M.

[Design of a dual-mode NoC router integrated with network interface for AMBA-based IPs](#)  
(2006) 2006 IEEE Asian Solid-State Circuits Conference, ASSCC 2006, art. no. 4197627, pp. 211-214.

Jou, J.M., Sun, C.-M., Wu, Y.-C., Lee, M.-C., Yan, Y.-X., Su, H.-Y., Yang, H.

[A multi-tile reconfigurable platform design for DSP applications](#)  
(2005) Proceedings of the Second IASTED International Multi-Conference on Automation, Control, and Information Technology - Signal and Image Processing, 2005, pp. 325-330.

Jeang, Y.-L., Jou, J.-M., Huang, W.-H.

[A binary tree based methodology for designing an application specific network-on-chip \(ASNOC\)](#)  
(2005) IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, E88-A (12), pp. 3531-3538.

Shiau, Y.-H., Jou, J.M., Liu, C.-C.

[Efficient architectures for the biorthogonal wavelet transform by filter bank and lifting scheme](#)

(2004) IEICE Transactions on Information and Systems, E87-D (7), pp. 1867-1877.

Shiau, Y.-H., Jou, J.M.

[A High-Performance Tree-Block Pipelining Architecture for Separable 2-D Inverse Discrete Wavelet Transform](#)

(2003) IEICE Transactions on Information and Systems, E86-D (10), pp. 1966-1975.

Jou, J.-M., Kuang, S.-R., Shiau, Y.-H., Chen, R.-D.

[Design of a dynamic pipelined architecture for fuzzy color correction](#)

(2002) IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 10 (6), pp. 924-929.

Chen, R.-D., Jou, J.-M.

[STG-level decomposition and resynthesis of speed-independent circuits](#)

(2002) IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 49 (12), pp. 1751-1763.

Jou, J.M., Shiau, Y.H., Zheng, B.R.

[A low power implementation for the motion estimation processor](#)

(2002) IEEE Region 10 Annual International Conference, Proceedings/TENCON, 1, pp. 220-223.

Jou, J.M., Shiau, Y.-H., Chen, P.-Y., Kuang, S.-R.

[A low-cost gray prediction search chip for motion estimation](#)

(2002) IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, 49 (7), pp. 928-938.

Jou, J.-M., Kuang, S.-R., Wu, K.-M.

[A hierarchical interface design methodology and models for SOC IP integration](#)

(2002) Proceedings - IEEE International Symposium on Circuits and Systems, 2, pp. II/360-II/363.

Jou, J.M., Shiau, Y.-H., Huang, C.-J.

[An efficient VLSI architecture for HMM-based speech recognition](#)

(2001) Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems, 1, pp. 469-472.

Kuang, S.R., Jou, J.M., Chen, R.D., Shiau, Y.H.

[Dynamic pipeline design of an adaptive binary arithmetic coder](#)

(2001) IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 48 (9), pp. 813-825.

Chen, P.-Y., Jou, J.M.

[An efficient blocking-matching algorithm based on fuzzy reasoning](#)

(2001) IEEE Transactions on Systems, Man, and Cybernetics, Part B: Cybernetics, 31 (2), pp. 253-259.

Jou, J.M., Shiau, Y.-H., Liu, C.-C.

[Efficient VLSI architectures for the biorthogonal wavelet transform by filter bank and lifting scheme](#)

(2001) Proceedings - IEEE International Symposium on Circuits and Systems, 2, pp. II529-II532.

Jou, J.M., Chen, P.-Y., Yang, S.-F.

[An adaptive fuzzy logic controller: Its VLSI architecture and applications](#)

(2000) IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 8 (1), pp. 52-60.

Chen, P.-Y., Jou, J.M.

[Adaptive arithmetic coding using fuzzy reasoning and grey prediction](#)

(2000) Fuzzy Sets and Systems, 114 (2), pp. 239-254.